Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

MPC993

The MPC993 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

FA SUFFIX
32–LEAD PLASTIC LQFP PACKAGE
CASE 873A–02

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control/Statis I/O
- 3.3V Operation
- 32–Lead LQFP Packaging
- ±50ps Cycle–Cycle Jitter

The MPC993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

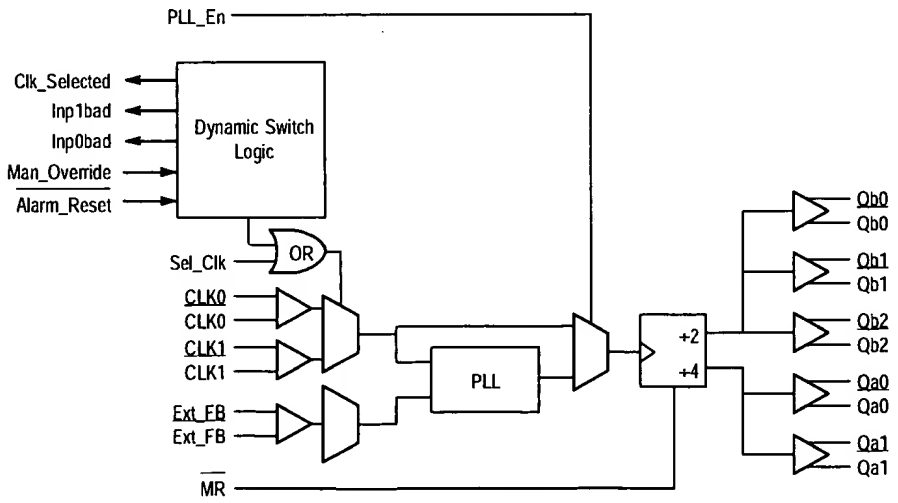

Figure 1. Block Diagram

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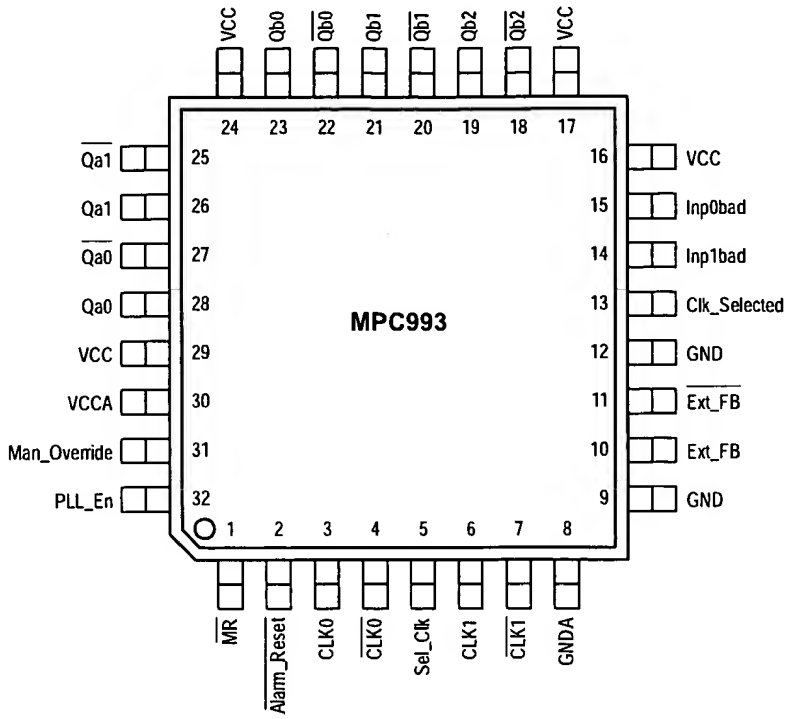


Figure 2. 32–Lead Pinout (Top View)

3.3V PECL DC Characteristics (T_A = –40°C to 85°C, V_{CC} = 3.3V ± 5%)

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (LVPECL Outputs) (50Ω to V_{CC} – 2.0V)	V_{CC} – 1.025		V_{CC} – 0.80	V
V_{OL}	Output LOW Voltage (LVPECL Outputs) (50Ω to V_{CC} – 2.0V)	V_{CC} – 1.80		V_{CC} – 1.60	V
V_{PP}	Input HIGH Voltage (LVPECL Inputs)	0.3		1.0	V
V_{CMR}	Input LOW Voltage (LVPECL Inputs)	1.0		V_{CC} – 0.6	V
V_{OH}	Output HIGH Voltage (LVCMOS Outputs)	2.4			V
V_{OL}	Output LOW Voltage (LVCMOS Outputs)			0.5	V
V_{IH}	Input HIGH Voltage (LVCMOS Inputs)	2.0		3.3	V
V_{IL}	Input LOW Voltage (LVCMOS Inputs)			0.8	V
I_{IL}	Input LOW Current	0.5			µA
I_{EE}	Power Supply Current GNDA GND		15 80	20 180	mA

3.3V PECL AC Characteristics (T_A = –40°C to 85°C, V_{CC} = 3.3V ± 5%) (Note 6.)

Symbol	Parameter		Min	Typ	Max	Unit
f_{VCO}	PLL VCO Lock Range (Note 5.)		200		360	MHz
t_{pwi}			25		75	%
t_{pd}	Propagation Delay (Note 1.)	CLKn to Q (Bypass) CLKn to Ext_FB (Locked (Note 2.))	1.7 –150	2.3 0	2.8 170	ns ps
t_r/t_f	Output Rise/Fall Time		200		800	ps
t_{skew}	Output Skew	Within Bank All Outputs			70 100	ps
Δ_{pe}	Maximum Phase Error Deviation				TBD (Note 3.) TBD (Note 4.)	ps
$\Delta_{per/cycle}$	Rate of Change of Periods	75MHz Output (Note 1., 3.) 150MHz Output (Note 1., 3.) 75MHz Output (Note 1., 4.) 150MHz Output (Note 1., 4.)		20 10 200 100	50 25 400 200	ps/ cycle
t_{pw}	Output Duty Cycle		45		55	%
t_{jitter}	Cycle–to–Cycle Jitter, Standard Deviation (RMS) (Note 1.)				20	ps
t_{lock}	Maximum PLL Lock Time				10	ms

1. Guaranteed, not production tested.
2. Static phase offset between the selected reference clock and the feedback signal.
3. Specification holds for a clock switch between two signals no greater than 400ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information section on page 4 for more detail)
4. Specification holds for a clock switch between two signals no greater than ±π out of phase. Delta period change per cycle is averaged over the clock switch excursion.
5. The PLL will be unstable using a ÷2 output as the feedback. Either one of the ÷4 outputs (Qa0 or Qa1) should be used as the feedback signal.
6. PECL output termination is 50 ohms to V_{CC} – 2.0V.

PIN DESCRIPTIONS

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 2x output pairs
Inp0bad	LVCMOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVCMOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVCMOS Output	'0' if clock 0 is selected, '1' if clock 1 is selected
Alarm_Reset	LVCMOS Input	'0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is "one–shotted" (50kΩ pullup)
Sel_Clk	LVCMOS Input	'0' selects CLK0, '1' selects CLK1 (50kΩ pulldown)
Manual_Override	LVCMOS Input	'1' disables internal clock switch circuitry (50kΩ pulldown)
PLL_En	LVCMOS Input	'0' bypasses selected input reference around the phase–locked loop (50kΩ pullup)
MR	LVCMOS Input	'0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50kΩ pullup)
VCCA	Power Supply	PLL power supply
VCC	Power Supply	Digital power supply
GNDA	Power Supply	PLL ground
GND	Power Supply	Digital ground

Applications Information

The MPC993 is a dual clock PLL with on–chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

Definitions

primary clock: The input CLK selected by Sel_Clk.
secondary clock: The input CLK NOT selected by Sel_Clk.
PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

Status Functions

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.
INP_BAD: Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm_Reset.

Control Functions

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.
Alarm_Reset: Asserted by a negative edge. Generates a one–shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.
PLL_En: While (L), the PLL reference signal is substituted for the VCO output.
MR: While (L), internal dividers are held in reset which holds all Q outputs LOW.

Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC993's, the following procedure should be used. Assuming that the input CLKs to all MPC993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC993 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

Hot insertion and withdrawal

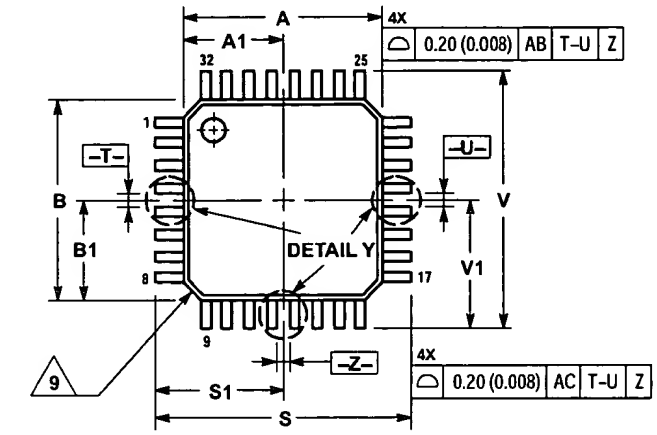
In PECL applications, a powered up driver will experience a low impedance path through an MPC993 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

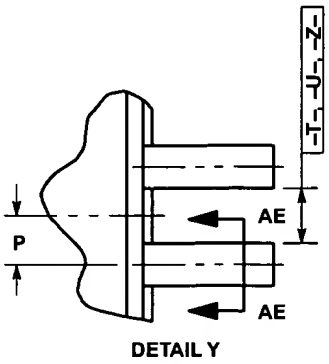
Acquiring Frequency Lock

1. While the MPC993 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De–assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

OUTLINE DIMENSIONS

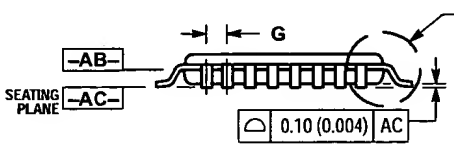
FA SUFFIX
PLASTIC LQFP PACKAGE
CASE 873A–02
ISSUE A

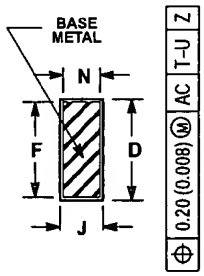




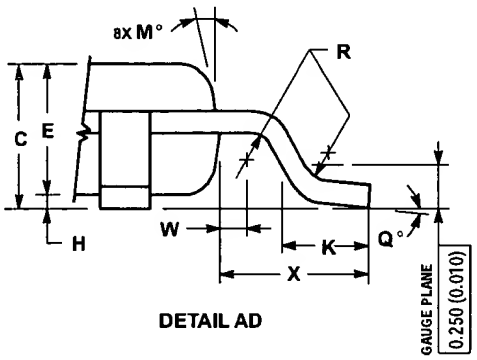
DETAIL Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -AB- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -T-, -U-, AND -Z- TO BE DETERMINED AT DATUM PLANE -AB-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -AC-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -AB-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.





SECTION AE–AE



DETAIL AD

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

NOTES

NOTES

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